and 12 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,384,455 to Nishigori; Claims 1-4 and 11 were rejected under 35 U.S.C. § 102(b)/103(a) as being unpatentable over U.S. Patent No. 5,519,243 to Kikuda et al.; Claims 13 and 14 were rejected under 35 USC 103(a) as being unpatentable over Nishigori n view of U.S. Patent No. 6,066,520 to Suzuki; and Claims 13 and 14 were rejected under 35 USC 103(a) as being unpatentable over Wei et al. in view of Sazuki.

Briefly recapitulating, the present invention (Claim 1) provides a semiconductor device including a first well at which a first active element is provided, a second well at which a second active element is provided, and a first conductive layer which electrically connects the first well and the second well.

Page 11 of the Office Action asserts that "Wei et al. teach in Figure 10B a first well 274 at which a first semiconductor element 246, 278 or 276 is provided, and a second well at which a second semiconductor element 268 or 246 is provided. A semiconductor element can be any element which is used in a semiconductor device." Claim 1 has been amended to define first and second active elements provided at first and second wells, respectively. Applicants respectfully submit that the elements relied upon in the office action are not active elements. Element 246 is an impurity layer. Element 278 is a field oxide which is an insulator. Lastly, element 276 is merely a doped region. That is, neither element 246, 276, or 278 is an active element. Consequently, Wei et al. are not believed to anticipate or render obvious the subject matter defined by Claim 1.

Likewise, Nishigohri fails to disclose "a first well at which a first active element is provided" as recited in claim 1. While an element formed of a transistor having a gate 33 and a diffusion layer 35 is provided at a well 31 in Nishigohri's Figure 16, an active element is not provided at region 41. The office action asserts that "a first semiconductor element 32... is provided." Applicants believe that the office action intended to identify element 33. In any

event, "gate electrode" 33 is not even provided in well 40. "Diffusion layer" 36 (also asserted in the Office Action) lies across the well, and "oxide film" 27 is a dielectric. Consequently, Nishigohri is not believed to anticipate or render obvious the invention of claim 1.

Kikuda et al. fail to disclose "a first conductive layer electrically connects the first well" as recited in amended claim 1. The wells 4 and 33 in Kikuda et al.'s Figure 3 are electrically separated from each other. Namely, the well 6 which the Office action asserts corresponds to the first conductive layer of the present invention is not electrically connected to the wells 4 and 33. Moreover, there is no suggestion of connecting the wells 4 and 33 by the well 6. This is due to the fact that there is no reason for connecting the wells 4 and 33 when different voltages V_{CC} and V_R are provided to the wells 4 and 33, respectively. Further, there is no motivation either to cause a short circuit between the power supply voltage V_{CC} (or V_R) and a ground voltage V_{SS} that develops when the well 6 connects the wells 4 and 33. Consequently, Kikuda et al. are not believed to anticipate the subject matter defined by claim 1.

In light of the above discussion, it is respectfully submitted that Claim 1 is patentably distinguishable from the applied patents and publication, and the dependent Claims 2-12 are therefore also patentably distinguishable from the applied patents and publication.

Regarding claims 13 and 14, they are believed to be allowable for at least the same reasons as Claim 1. Hence, claims 13 and 14 are also believed to be in condition for allowance.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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IN THE CLAIMS

Please amend Claims 1 and 13 as follows:

1. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate;

a first well of a prescribed conductivity type at which a first [semiconductor] active element is provided, said first well being selectively formed in a surface of said semiconductor substrate;

a second well of the same conductivity type as said prescribed conductivity type at which a second [semiconductor] active element is provided, said second well being selectively formed in said surface of said semiconductor substrate;

a first conductive layer across said first well and said second well in said surface of said semiconductor substrate with an end provided on said first well and another end provided on said second well, said first conductive layer electrically connecting said first well and said second well; and

a first contact electrically connected with said first well.

13. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a first well of a prescribed conductivity type selectively formed in a surface of said semiconductor substrate and including a first active element;

a second well of the same conductivity type as said prescribed conductivity type selectively formed in a surface of said semiconductor substrate and including a second active element;

a conductive layer across said first well and said second well in said surface of said semiconductor substrate with an end provided on said first well and another end provided on said second well, said conductive layer including a compound layer of the material for said semiconductor substrate and a metal; and

a first contact electrically connected with said first well.